REMARKS

Claims 3 and 4 stand objected to under 37 CFR 1.75 (MPEP 706.03(k)) for duplicate claiming. Claims 3 and 4 have been amended herein and new claims 5 - 7 have been added.

The invention is a capacitor which is attached to the voltage supply terminal of a semiconductor device which device is mounted onto a PC board. The capacitor shunts voltage fluctuations (voltage spikes) to ground. These spikes are created internal to the circuitry by the fast switching times of the circuitry. These spikes are not external noise generated. The circuit of the present invention is not concerned with shielding from external noise.

The invention creates the subject capacitor from a co-axial cable structure wherein the "wire" at the core of the co-ax cable is in fact the connection/wire to the semiconductor device, itself. This co-ax cable is passed through a hole in the PC board to come in contact with the semiconductor device. One element of the capacitor is the actual "wire" being connected to the semiconductor device terminal, which wire passes through the hole or "via" in the PC board. The other element of the capacitor is an outer conductive coating/sheath which is in a press fit with an exposed ground plane transecting the hole. There is no soldering or welding of the connection of the outer co-ax element with the PC board ground plane. The electrical connection between the outer element of the capacitor and the exposed ground plane in the hole is made with a press fit. The two elements of the capacitor are separated by a high dielectric constant material.

Claim 3 recites a method of making a semiconductor package with a voltage fluctuation suppressing capacitor connected on a terminal of a semiconductor device mounted on a circuit board, wherein a coaxial capacitor is press fit into a hole in the board to which the semiconductor device is to be mounted. One element of this capacitor (the core conductor wire) is the actual conductor wire which is connected directly to a terminal of the semiconductor

device, while the other element (the conductive outer sheath) is press fitted against a grounded plane in the board to make that electrical connection.

Claim 4 recites a method of making the semiconductor package with the same voltage fluctuation suppression capacitor. However, the steps differ from claim 3 in that the inside of the hole in the board is first coated with a conductive layer in contact with the grounded plane. A conductor wire coated with a high dielectric constant material is then press fit into the coated hole.

While the product produced by the method of claims 3 and 4 is substantially the same coaxial capacitor, the order in which the steps are conducted varies between the two claims and therefore there can be no duplicate claiming.

Claims 3 and 4 stand rejected under 35 USC 102(e) as anticipated by Chang, US 20020017399. To anticipate the method claims of the present invention, the reference must teach the same steps in the same order. It does not and therefore the § 102(e) rejection is respectfully TRAVERSED.

Not only does the Chang reference not teach the process of the present invention, the resultant product is different.

Chang teaches a method of shielding a conductor wire (not shown) from outside noise. To do this he builds a shield from a cylindrical conductor 404, 612, which has dielectric material 406, 608, surrounding the respective cylinder 404, 612, and an outer conductive cylinder 402, 606 in turn surrounding the dielectric material. The inner cylinder is connected to one supply terminal such as a positive voltage, and the outer cylinder is connected to another supply terminal such as a negative voltage. Neither of Chang's cylinders are intended to be connected to the semiconductor. Neither of Chang's cylinders are intended to act a conductor carrying a signal to the semiconductor. In fact, they cannot, as they would loose their shielding function.

Chang chooses the value of his dielectric material 406, 608 to create a capacitor to

ground (negative voltage) or a resistor for his shielding. This selection will depend upon other circuit factors and the frequencies of the outside noise from which Chang wishes to shield his signal line to his semiconductor. The interior of Chang's device is hollow, to act as a via, as Chang's actual signal carrying wire must pass there through.

Chang does not concern himself with press fitting an assembled cable into his hole. Specifically, the steps of Chang's manufacturing process are: (a) forming a first hole in a carrier board; (b) making the interior of the hole conduct electricity to form an outer cylinder-shaped conductor; placing an insulating material in the outer cylindrical conductor to form an insulating fill; (c) forming a second hole in the insulating fill; and making the interior of the second hole conduct electricity to form an inner cylinder-shaped conductor.

Chang drills two holes. A first hole is drilled through his PC board. A second hole is drilled through the dielectric material that is formed into the hole after the hole in the PC board is plated with a conductive material to form the outer cylinder. The second inner hole is then plated to with the conductive material to form the inner cylinder.

Applicant forms but one hole through his PC board. Applicant's PC board hole is plated to form the outer conductive cylinder of applicant's capacitor. Then applicant's dielectric covered conductor wire is press fit into the plated hole. Applicant does not have an inner conductive cylinder which would be necessary for a shield, as applicant is not making a capacitive shield nor is applicant making a resistor shield. Applicant is not concerned with outside noise and he does not shield his semiconductor device conductor wire from any outside noise. Applicant's press fit not only completes the electrical connection with the ground plane exposed surface, but also assures the precise distance between the two elements of the capacitor over the entire length of its extension through the board hole.

Contrary to the prior art, applicant is concerned with shunting to ground any transient peaks in the conductor wire to his semiconductor device and not with shielding that conductor wire from outside signals.

Applicant also assembles his capacitor into his PC board in a single step after assembling the complete capacitor cable outside of the PC board. Again, applicant is concerned with a press fit into the PC board hole in order to make the electrical connection with the . Again, applicant is concerned with an inner conductor wire being the actual conductor connected to the semiconductor device terminal point. Again, the press fit not only assures good electrical contact with the exposed surface of the ground plane in the hole, but also assures the precise consistent straight shape of the co-axial capacitor throughout the length of the hole and maintains a precise distance between the two elements of the capacitor over the entire length of its extension through the board hole.

The claimed process of claims 3 and 4 drastically departs from the process taught by Chang. Applicant's resultant product drastically departs from Chang's product. The purpose and operation of applicant's resultant product departs from the purpose and operation of Chang's product.

New claims 5 - 7 recite the present invention in other degrees of scope.

It is requested that the application be re-examined with the claims 3 - 7 presented herein above. It is further requested that these claims be determined to distinguish the present invention over the prior art. This application should now be allowed to pass to issue.

Respectfully submitted,
Paul & Paul

Date: 09/07/05

by: John J. Simkanich
Regis. No. 26,036
2900 Two Thousand Market Street
Philadelphia, PA 19103

(215) 568-4900
FAX 215-567-5057

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on Sept 7, 2005
(date)

PAUL & PAUL
by: John J. Simkanich

(signature)